Claim Listing

Please cancel claims 9, 11, 12, 15, 20, 24, 26, 27, and 30.

1. (Currently Amended) An apparatus for computing a result of a floating-point operation[[s]], wherein the apparatus receives an aligned addend comprising a plurality of bits and ~~receives~~ a plurality of products, the apparatus comprising:

a compound incrementer~~, wherein the compound incrementer~~ coupled to receive[[s]] at least some of the plurality of bits of the aligned addend and a control signal, and configured to produce an output dependent upon the received bits of the aligned addend and the control signal;

a compression counter~~, wherein the compression counter~~ coupled to receive[[s]] at least some of the plurality of bits of the aligned addend and the products and configured to produce an output dependent upon the received bits of the aligned addend and the received products;

a compound adder [[that]] coupled to receive[[s]] the output of the compression counter and configured to produce an output dependent upon the output of the compression counter;

a carry network~~, wherein the carry network simultaneously computes an end-around-carry with at least some other computational operations and wherein the carry network receives the products and receives the output of the compression counter~~ coupled to receive sign bits of the products and the output of the compression counter and configured to produce an output signal and a carry signal dependent upon the received sign bits of the products and the received output of the compression counter;

a selector~~, wherein the selector at least~~ coupled to receive~~s the output of~~ at least some of the plurality of bits of the aligned addend and ~~wherein the selector al least receives the output of the carry network~~ the output signal and the carry signal produced by the carry network, wherein the selector is configured to produce a selection signal dependent upon the received bits of the aligned addend, the received output signal, and the received carry signal; and

a plurality of multiplexers (muxes)~~, wherein the plurality of muxes~~ coupled to receive ~~outputs from~~ the output of the compound incrementer, the output of the compound adder, and the selection signal produced by the selector, and configured to produce the result by selecting between the received output of the compound incrementer and the received output of the compound adder dependent upon the selection signal produced by the selector.

2. (Currently Amended) The apparatus of Claim 1, wherein the compound incrementer further comprises:

an incrementer coupled to receive at least some of the plurality of bits of the aligned addend and configured to produce an output dependent upon the received bits of the aligned addend and the control signal; and

a plurality of negation devices.

3. (Currently Amended) The apparatus of Claim 2, ~~further comprising the output of the incrementer inputs into at least one negation device of the plurality of negation devices~~ wherein one of the negation devices is coupled to receive the output of the incrementer and the control signal,

and is configured to produce an output dependent upon the received output of the incrementer and the control signal.

4. (Currently Amended) The apparatus of Claim [[3]] 2, wherein the plurality of negation devices ~~are XOR-gates~~ implement exclusive-OR (XOR) logic functions.

5. (Original) The apparatus of Claim 2, wherein the plurality of negation devices are XOR-gates.

6. (Currently Amended) The apparatus of Claim 1, wherein the carry network further comprises:

~~an XOR-gate~~ logic coupled to receive the sign bits of the products and configured to produce the output signal dependent upon the received sign bits of the products; and

a carry generator coupled to receive the output of the compression counter and configured to produce the carry signal dependent upon the received output of the compression counter.

7. (Currently Amended) The apparatus of Claim [[4]] 1, wherein the carry network further comprises:

an XOR-gate coupled to receive the sign bits of the products and configured to produce the output signal dependent upon the received sign bits of the products; and

a carry generator coupled to receive the output of the compression counter and configured to produce the carry signal dependent upon the received output of the compression counter.

8. (Currently Amended) The apparatus of Claim 1, wherein the ~~carry network and the~~ selector ~~are at least~~ is configured to ~~utilize a portion of the aligned addend to precompute a plurality of sets of~~

~~select signals~~ produce a plurality of selection signals dependent upon the received bits of the aligned addend, the received output signal, and the received carry signal.

9. (Canceled).

10. (Currently Amended) The apparatus of Claim 1, wherein the output of the compound adder comprises a sum signal and an incremented sum signal, and one ~~mux~~ of [[a]] the plurality of muxes is ~~at least configured~~ coupled to receive [[a]] the sum signal from the compound adder, [[an]] the incremented sum signal from the compound adder, and an inverted version of the sum signal ~~from the compound adder producing~~ , and is configured to produce at least a portion of ~~an adder~~ the result.

11. (Canceled).

12. (Canceled).

13. (Original) The apparatus of Claim 1, wherein the compression device further comprises a 3:2 Counter.

14. (Original) The apparatus of Claim 4, wherein the compression device further comprises a 3:2 Counter.

15. (Canceled).

16. (Currently Amended) A computer program product for computing a result of a floating-point operation[[s]], wherein the computer program product receives an aligned addend comprising a plurality of bits and ~~receives~~ a plurality of products, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

~~a computer program product~~ computer readable program code means for operating as a compound incrementer, wherein the compound incrementer receives at least some of the plurality of bits of the aligned addend and a control signal, and produces an output dependent upon the received bits of the aligned addend and the control signal;

~~a computer program product~~ computer readable program code means for operating as a compression counter, wherein the compression counter receives at least some of the plurality of bits of the aligned addend and the products and produces an output dependent upon the received bits of the aligned addend and the received products;

~~a computer program product~~ computer readable program code means for operating as a compound adder that receives the output of the compression counter and produces an output dependent upon the output of the compression counter;

~~a computer program product~~ computer readable program code means for operating as a carry network, wherein the carry network ~~simultaneously computes an end-around-carry with at least some other computational operations and wherein the carry network receives the products and received the output of the compression counter~~ receives sign bits of the products and the output of the compression counter and produces an output signal and a carry signal dependent upon the received sign bits of the products and the received output of the compression counter;

~~a computer program product~~ computer readable program code means for operating as a selector, wherein the selector ~~at least~~ receives ~~the output of~~ at least some of the plurality of bits of the aligned addend and ~~wherein the selector at least receives the output of the carry network~~ the output signal and the carry signal produced by the carry network, and wherein the selector produces a selection signal dependent upon the received bits of the aligned addend, the received output signal, and the received carry signal; and

~~a plurality of computer program products~~ computer readable program code means for operating as a plurality of multiplexers (muxes), wherein the plurality of muxes receive ~~outputs from~~ the output of ~~the computer program products operating as~~ the compound incrementer, the output of the compound adder, and the selection signal produced by the selector, and produce the result by selecting between the received output of the compound incrementer and the received output of the compound adder dependent upon the selection signal produced by the selector.

17. (Currently Amended) The computer program product of Claim 16, wherein the ~~computer program product~~ computer readable program code means for operating as compound incrementer further comprises:

~~a computer program product~~ computer readable program code means for operating as an incrementer, wherein the incrementer receives at least some of the plurality of bits of the aligned addend and produce an output dependent upon the received bits of the aligned addend and the control signal; and

~~a plurality of computer program products~~ computer readable program code means for operating as a plurality of negation devices.

18. (Currently Amended) The computer program product of Claim 17, ~~further comprising the output of the computer program product operating as incrementer inputs into at least one computer program product operating as negation device of the plurality of a computer program products operating as negation devices~~ wherein one of the negation devices receives the output of the incrementer and the control signal, and produces an output dependent upon the received output of the incrementer and the control signal.

19. (Currently Amended) The computer program product of Claim [[18]] 17, wherein the ~~plurality of computer program products~~ computer readable program code means for operating as the plurality of negation devices ~~are computer program products operating as XOR gates~~ comprises computer readable program code means for implementing exclusive-OR (XOR) logic functions.

20. (Canceled).

21. (Currently Amended) The computer program product of Claim 16, wherein the ~~computer program product~~ computer readable program code means for operating as the carry network further comprises:

~~a computer program product~~ computer readable program code means for operating as ~~an XOR gate~~ logic receiving the sign bits of the products and producing the output signal dependent upon the received sign bits of the products; and

~~a computer program product~~ computer readable program code means for operating as a carry generator, wherein the carry generator receives the output of the compression counter and produces the carry signal dependent upon the received output of the compression counter.

22. (Currently Amended) The computer program product of Claim [[19]] 16, wherein the ~~computer program product~~ computer readable program code means for operating as carry network further comprises:

~~a computer program product~~ computer readable program code means for operating as an XOR-gate, wherein the XOR-gate receives the sign bits of the products and produces the output signal dependent upon the received sign bits of the products; and

a ~~computer program product~~ computer readable program code means for operating as a carry generator, wherein the carry generator receives the output of the compression counter and produces the carry signal dependent upon the received output of the compression counter.

23. (Currently Amended) The computer program product of Claim [[21]] 16, wherein the ~~computer program products operating as the carry network and the~~ selector ~~are at least configured to utilize a portion of the aligned addend to precompute a plurality of sets of select signals~~ produces a plurality of selection signals dependent upon the received bits of the aligned addend, the received output signal, and the received carry signal.

24. (Canceled).

25. (Currently Amended) The computer program product of Claim 16, wherein ~~one computer program product operating as mux of a plurality of computer program products operating as muxes is at least configured to receive a sum signal from the computer program products operating as the compound adder, an incremented sum signal from the computer program products operating as the compound adder, and an inverted sum of the computer program products operating as the compound adder producing at least a portion of an adder result~~ the output of the compound adder comprises a sum signal and an incremented sum signal, and one of the plurality of muxes is coupled to receive the sum signal from the compound adder, the incremented sum signal from the compound adder, and an inverted version of the sum signal, and is configured to produce at least a portion of the result.

26. (Canceled).

27. (Canceled).

28. (Currently Amended) The computer program product of Claim 16, wherein the ~~computer program product~~ computer readable program code means for operating as compression device further comprises ~~a computer program product~~ computer readable program code means for operating as 3:2 Counter.

29. (Currently Amended) The computer program product of Claim 19, wherein the ~~computer program product~~ computer readable program code means for operating as compression device

further comprises ~~a computer program product~~ computer readable program code means for operating as 3:2 Counter.

30. (Canceled).